Renumbered Claims

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24. A method of forming a vertical MOSFET, comprising the steps of:

forming a base region of second conductivity type in a semiconductor substrate having a drift region of first conductivity type therein that forms a P-N junction with the base region;

forming a source region of first conductivity type in the base region;

forming a deep trench having a first sidewall that extends adjacent the base region, in the semiconductor substrate;

lining the deep trench with a first electrically insulating layer;

refilling the lined deep trench with a trench-based source electrode;

selectively etching the trench-based source electrode to define a shallow trench therein and expose a first portion of the first electrically insulating layer that extends on the first sidewall of the deep trench;

selectively etching the first portion of the first electrically insulating layer to expose an upper portion of the first sidewall of the deep trench and reveal the base region;

lining the shallow trench with a gate insulating layer that extends on the exposed upper portion of the first sidewall of the deep trench and a bottom and sidewalls of the shallow trench;

forming a gate electrode that extends on a surface of the semiconductor substrate and extends into the lined shallow trench; and

forming a surface source electrode that electrically connects the trench-based source electrode, source region and base region together.

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25. The method of claim 24, wherein said step of forming a surface source electrode is preceded by the steps of:

forming a blanket passivation layer on the semiconductor substrate; and

patterning the blanket passivation to define contact holes therein that expose the trench-based source electrode, source region and base region.

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26. The method of claim 24, wherein the trench-based source electrode comprise polycrystalline silicon; and wherein said step of lining the shallow trench comprises thermally oxidizing the exposed upper portion of the first sidewall at a first rate and the bottom and sidewalls of the shallow trench at a second rate that is higher than the first rate.

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27. The method of claim 26, wherein said thermally oxidizing step comprises thermally oxidizing an upper surface of the trench-based source electrode to define a surface oxide layer thereon; and wherein said step of forming a surface source electrode is preceded by the step of selectively etching a portion of surface oxide layer extending adjacent the gate electrode to expose a portion of the upper surface of the trench-based source electrode.

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28. The method of claim 24, wherein said step of lining the shallow trench comprises thermally oxidizing the exposed upper portion of the first sidewall at a first rate and the bottom and sidewalls of the shallow trench at a second rate that is at least about equal to the first rate.

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29. A method of forming a vertical MOSFET, comprising the steps of:

forming a semiconductor substrate having therein a drift region, a transition region on the drift region, a base region on the transition region and a source region on the base region;

forming a deep trench having a first sidewall that extends adjacent the base, transition and drift regions, in the semiconductor substrate;

forming a trench-based source electrode in the deep trench;

forming a shallow trench that exposes the base region and source region extending along the first sidewall, in the trench-based source electrode;

forming a gate oxide insulating layer on the exposed base region;

forming a gate electrode that extends on an upper surface of the semiconductor substrate and extends into the shallow trench; and

forming a surface source electrode that electrically connects the trench-based source electrode, source region and base region together.

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30. The method of claim 28, wherein said step of forming a surface source electrode is preceded by the steps of:

forming a blanket passivation layer on the semiconductor substrate; and

patterning the blanket passivation to define contact holes therein that expose the trench-based source electrode, source region and base region.

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~~31~~. The method of claim ~~29~~, wherein said step of forming a gate electrode comprises forming multiple stripe-shaped gate electrodes that extend across the trench-based source electrode in a direction orthogonal to a lengthwise direction of the deep trench; and wherein the surface source electrode electrically connects the trench-based source electrode, source region and base region at locations extending between the multiple stripe-shaped gate electrodes.

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~~32~~. The method of claim ~~29~~, wherein the trench-based source electrode is separated from the first sidewall by a first electrically insulating layer; and wherein said step of forming a shallow trench comprises selectively etching a portion of the first electrically insulating layer exposed by the shallow trench using the trench-based source electrode as an etching mask.